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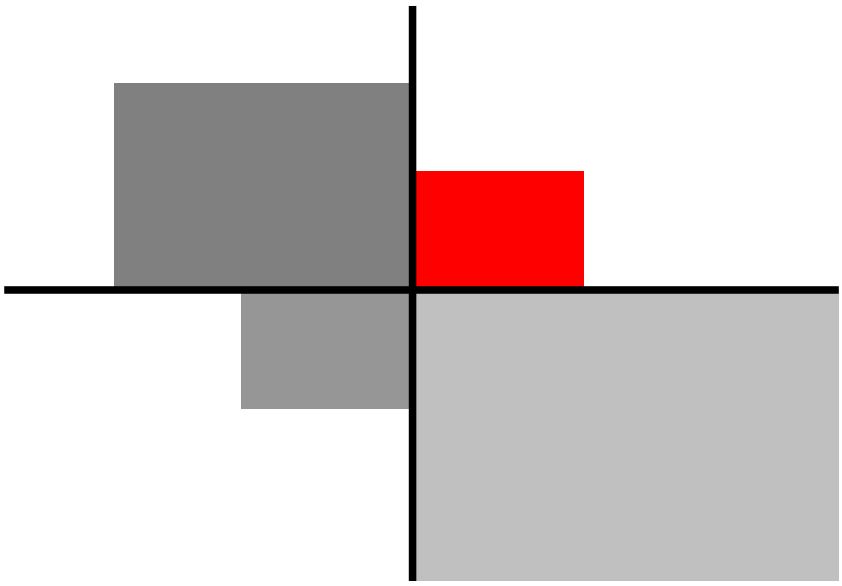
# Application Note AN-1402

## FPGA/CPLD Control System Integration for

## Sovereign Forager Autonomous Robotic Vehicle



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# FPGA/CPLD Control System Integration for

# Sovereign Forager Autonomous Robotic Vehicle

By William Lovell

## Introduction

Sovereign Forger Autonomous Robotic Vehicle (SFARV or Forager) is the medium weight Omni-chassis from c-Link Systems (cLS) Sovereign ARV product line. Forager uses a distributive process and control system based on FPGAs and CPLDs. The Application Note looks at "the big picture" of the inclusive system. Later Application Notes will be involved with the specifics of certain processors and their function within the system and its integration.

## Overview

The SFARV utilizes primarily FPGAs with CPLDs managing function specific jobs. Both parts were selected from Altera, Inc.; the FPGAs were selected from the Cyclone III family while the CPLDs are from the MAX IIG family. The product selection was based on ease of software use, density to cost, availability and power consumption.

The overall control system core contains a minimum of six FPGA based cards with a maximum of twelve. Each processor cards has an aluminum cooling and protection frame. These frames are then mounted in a stack and sealed together.

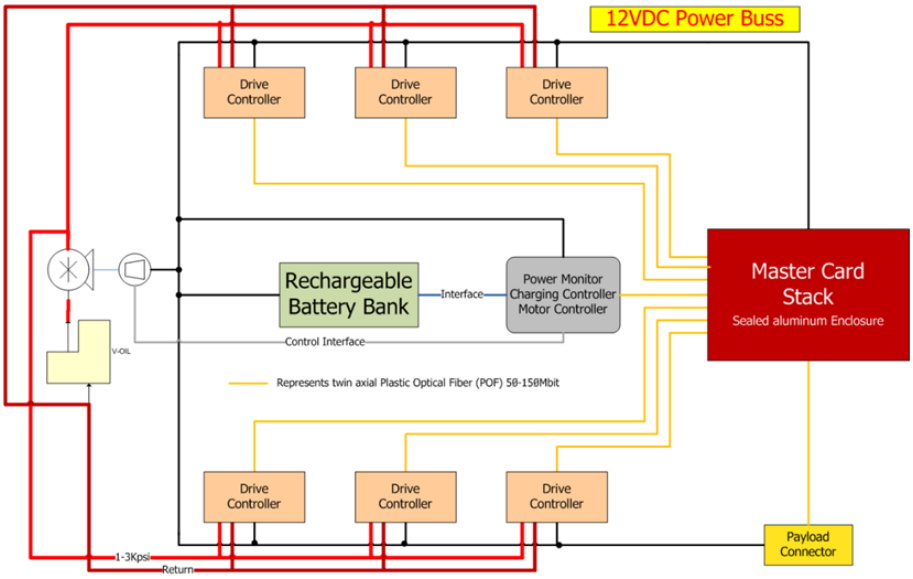


Figure 1 System Overview

At the writing of this note there were 18 CPLDs used in various tight control sections and the intelligent hydraulic valves. Refer to Figure 1 for broad outline and interconnection.

## Master controller (MC)

This is the mind and nervous system of the SFARV Omni-chassis. Within this aluminum sandwich resides six to twelve modules each containing a Cyclone III part.

Figure 2 depicts the basic requirements for the SFARV and other Omni-chassis. There are a few things different from conventional commercial vehicle controls;

1. A redundant processor
2. Message passing between the processor modules
3. Built-in test bus for field usage

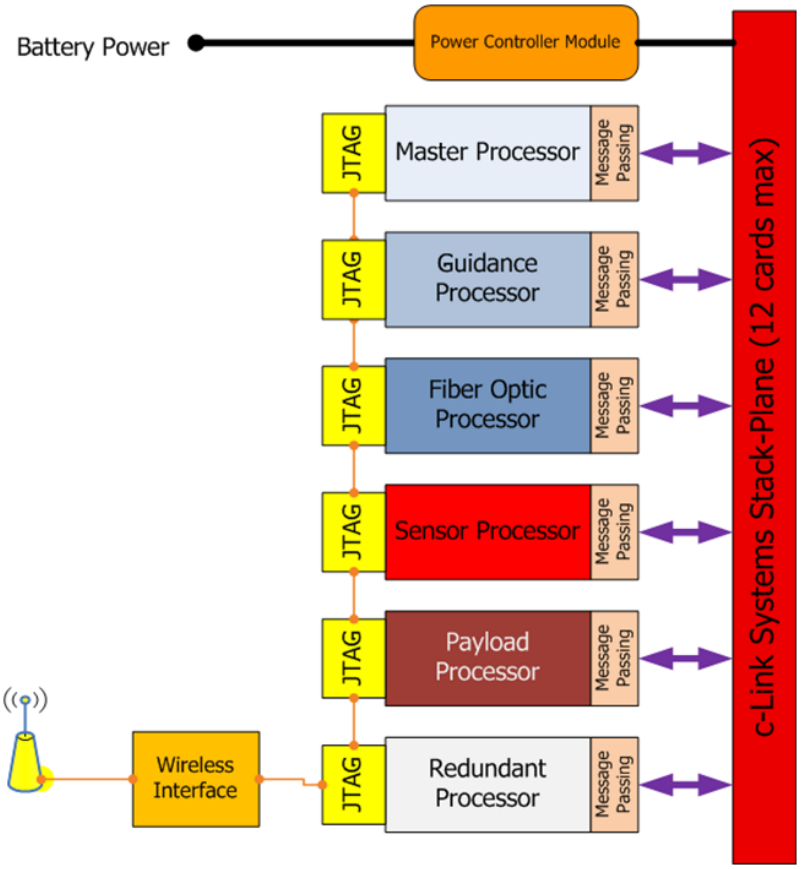


Figure 2 Master Controller

Each Cyclone III based module contains at least one Nios II 32-bit soft core processor from Altera. In some cases there are two to four of the Nios IIs with-in the part. This illustrates the versatility of the part and an additional motive for the part selection. By utilizing a single configurable component product production can be simplified. A tremendous feature that is inadequately used is the ability to dynamically reconfigure the Cyclone III. The reconfiguration could encompass the addition of hardware comparators temporarily. Energy conservation could also be derived reconfiguration along with simplified application code. Each module contains supporting application code flash, SRAM for working memory and FPGA configuration SEPROM. The exception to this is the Payload Processor, this unit has a SEPROM for configuration but it resides on the payload package. The reason for this unique action is the ability to swap out payload functions, in the field, exclusive of requiring reprogramming of the Master Controller. The payload module also contains the application code for the

Payload Processor and the Master Processor, thus alleviating the need to plug into the Forager or add a flash memory card. Application code required parameters are transferred via a wireless connection from a PC, laptop or potentially a PDA where the customer configuration program resides.

The MC is based upon c-Link Systems' "Stack-Plane". A Stack-Plane is the methodology utilized to interconnect the modules. This is accomplished with stackable connectors on each module, allowing for a vertical connection. The Stack-Plane is configured so that module position/ relationship to another module is immaterial. This style of backplane removes the need for a separate card that acts as the interconnection carrier. An enhancement to this construct is the use of synchronous message passing. c-Link uses message passing to create a deterministic communications bus structure. The informational transfer rate (packet rate) on the Stack-Plane is 8ØMB/s which allows for head room on expansion and higher traffic. Another distinctive function of the Master Controller is the built-in JTAG (IEEE 1149.1) bus. Augmented to the presence of the JTAG bus is the fact that it is connected to the outside world via a wireless module. This enhancement allows for monitoring and fault diagnostics prior to opening the Forager's panels. More detailed application notes on the Stack-Plane and JTAG implementation will be available at a later date.

## Master Processor (MP)

The Master Processor does what the named signifies; it is the overall controlling module tasked with the responsible for the final decision and action. MP contains two to four Nios II processors with supporting flash and work memory (SRAM), see Figure 3.

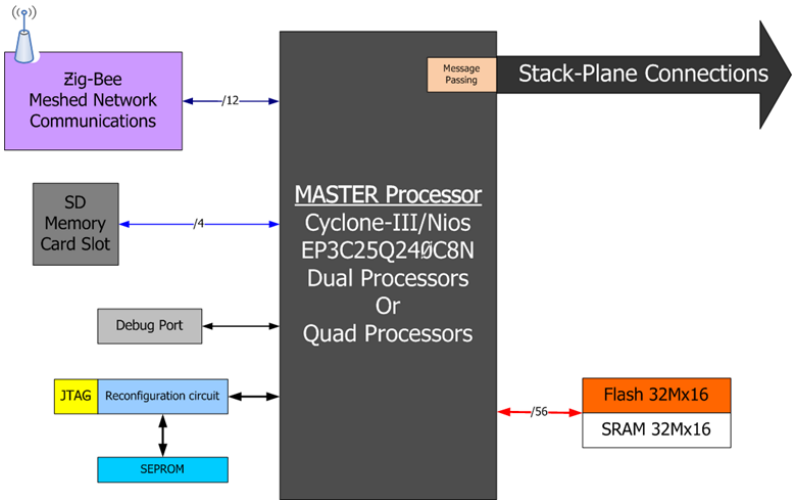


Figure 3 Master Processor

The Zig-Bee communications section contained on the module has a dedicated Nios II processor. The Nios II is utilized for packet control, data movement and all-around housekeeping.

To assist the customer with repetitive jobs or functions an SD Memory card slot has been included on the Master Processor module. To access this plug-in the front cover will have to be removed.

## Guidance Processor (GP)

The Guidance Processor is the second most important module it is surpassed only by the Master Processor. An ARV is ineffective if it can not determine what the current location/position is and extrapolate where it has been or going too. This scenario likens to the old fashion child's toy that runs along the floor until it bumps an object then changes direction. An ARV that is rolling along till it encounters an object and either changes direction or stops has very limited use and could pose as a receipt for disaster.

The GP in the SFARV is a moderately complex system module containing a basic Inertial Measurement Unit (IMU) and two GPS receivers, see Figure 4. The antennas for the GPS units are mounted on the top deck left and right sides. Bonus of two GPS units is the ability to confirm left/right tilt. The Inertial Measurement Unit is illustrated in a disassembled visual aspect. The basic IMU will contain a 3-axis accelerometer and a Yaw (Z-axis) rate gyro. The full IMU contain rate gyros on the roll (X) and pitch (Y) axis.

Like the other modules the Guidance Processor, it contains separate external flash and SRAM. From a customer view this module and its functions are buried with no interaction required. From a software view this module contains the Kalman Filtering to predict path motion. Kalman Filtering is an efficient recursive filter that estimates the state of a dynamic system from a series of incomplete and noisy measurements.

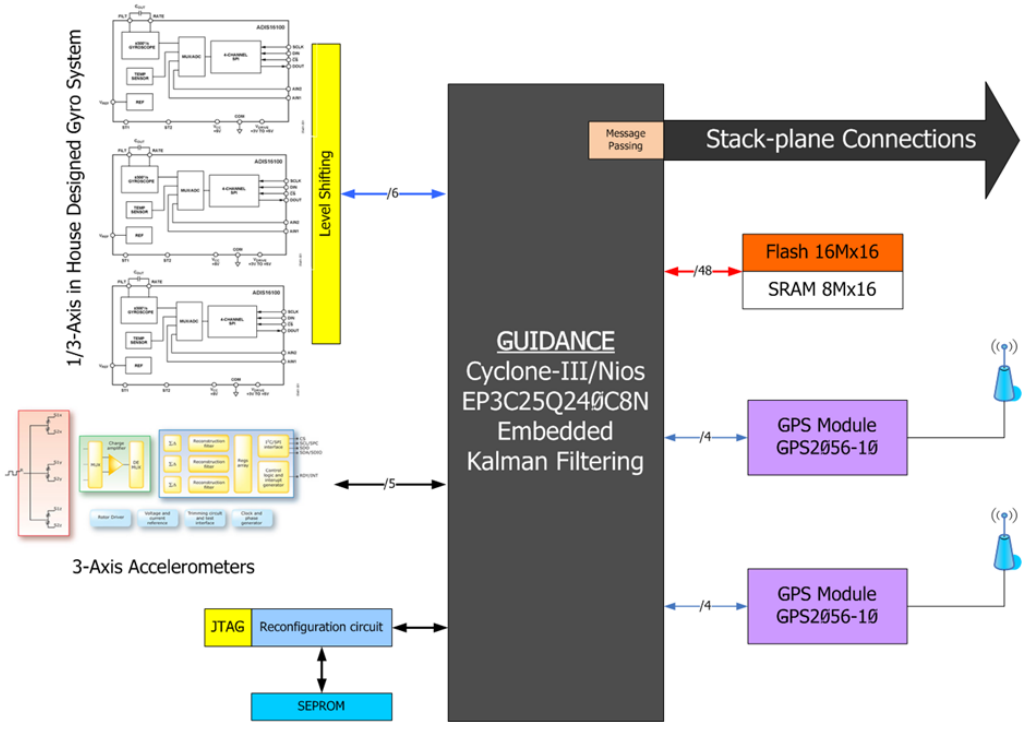


Figure 4 Guidance Processor

## Fiber optic processor (FOP)

Within the SFARV and the other Omni-chassis's the Fiber Optic Processor module is the guru of communications, see Figure 5. This module has twelve bi-directional fiber optic connections. Each of these connections has the ability to be powered down to reduce power consumption. The bi-directional channels can be used as individual transmitter or receiver. Each channel communicates independently but can also be grouped together for a broadcast mode. Current data transfer rate is at 1ØØMb/s, this limitation is based on the selected Cyclone IIIs clocking speed. Moreover if a higher speed part selected an increased transfer rate could result. With the longest fiber run being ten feet, deployment of low cost Plastic Optical Fiber (POF) can be realized. POF was selected for the associated cost and ease of install; there are no costly connectors or equipment for connector install.

Each channel on the FOP has the ability to run at a different data rate. These concept allows for the mix of different data rate modules with in the Omni-chassis, allows for power saving measures and less current to the LED for transmission. The actual transfer protocol is based on 8B/1ØB which assists in the synchronization and reduction of lost packet data. Communications is also confined to a fixed packet construct. As with the Stack-Plane by fixing the packet size the transfer at all times is deterministic.

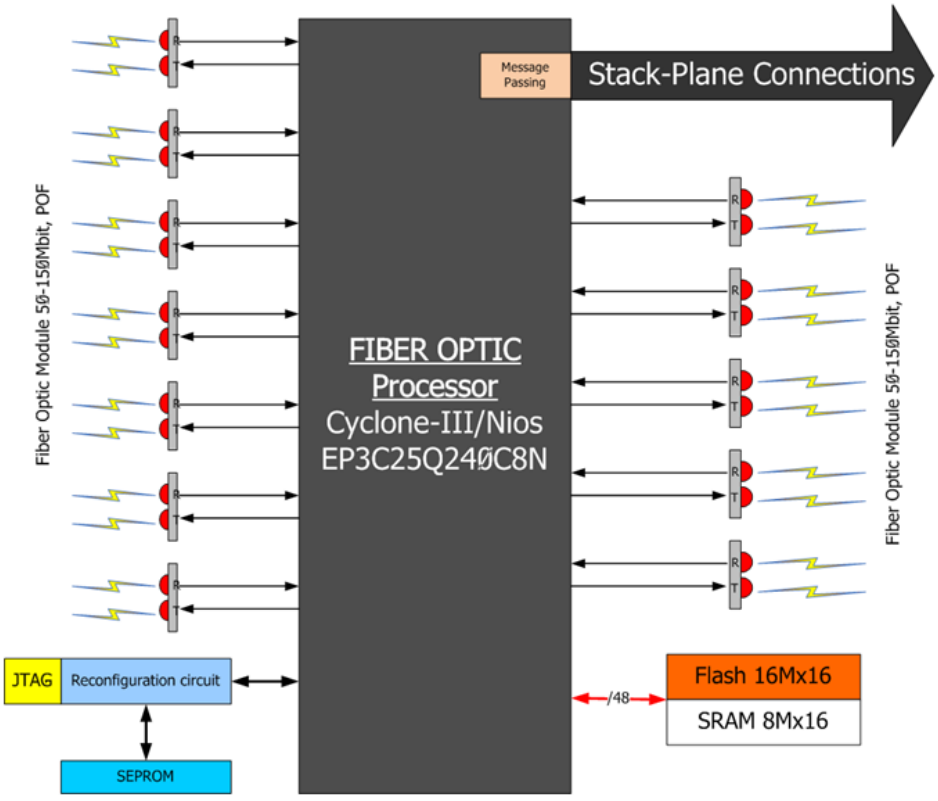


Figure 5 Fiber Optic Processor

An example of the broadcast action would be the setup and command to move forward. First broadcast packet contains the needed parameters; direction, rate and bypass/active. Second packet basically says "GO".

## Sensor Processor (SP)

Sensor Processor module interprets the incoming data from the sensor suites (electronic eyes and ears) surrounding the SFARV, see Figure 6. The incoming data is processed and compared against parameters received from the Master Processor. The SP's function appears at first glance to be backwards, if a data segment is within the parameter range the SP notifies the MP and the data is transferred. It is then the Master Processor's function to decide what if anything to do with the information.

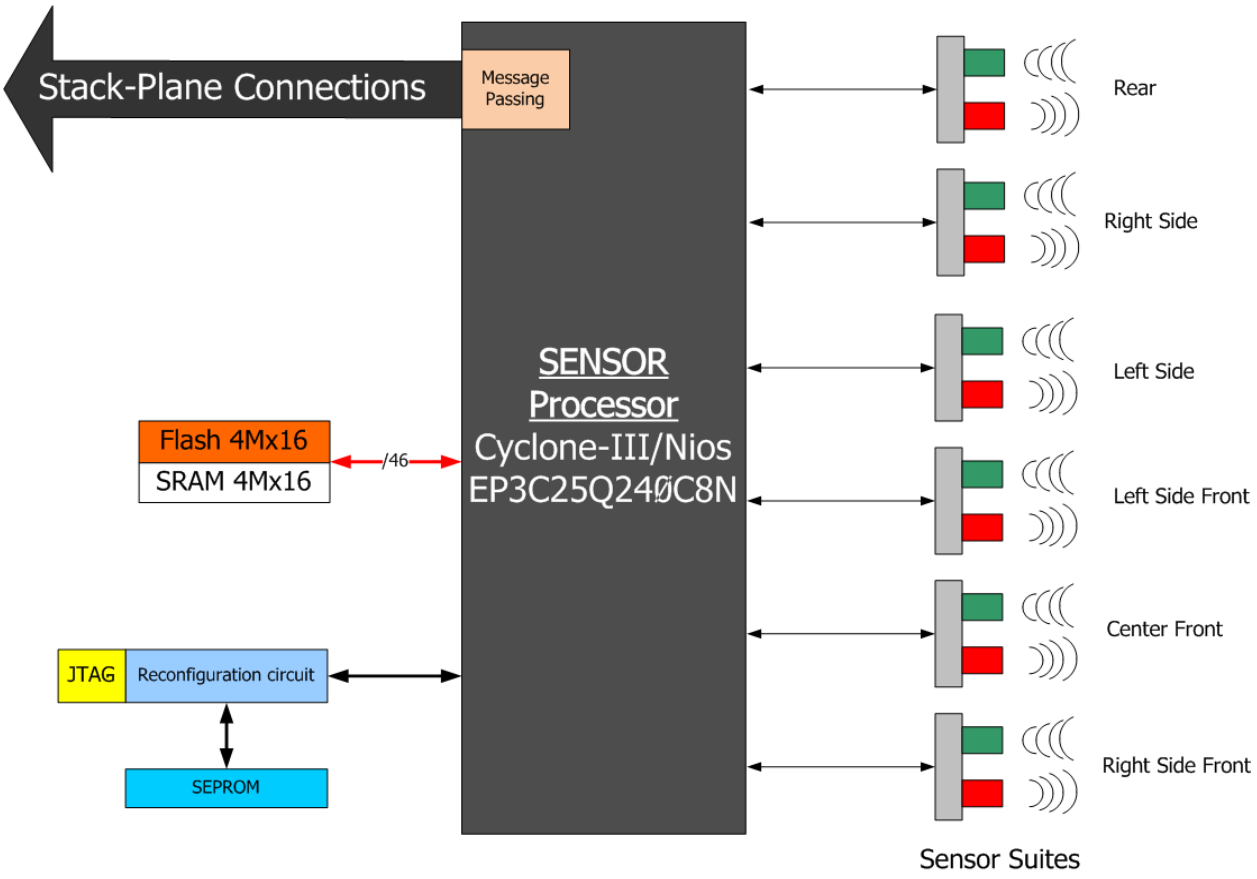


Figure 6 Sensor Processor

The sensor suites are attached through high speed POF which is inline with the other systems and their connections within the chassis. The sensor suite consists of both medium and close range sensing. One safety measure is lower end of the medium range overlaps the high end of the short range sensor. This maintains a constant image margin and assists in the prevention of accidents. The medium range sensor is an ultra-sonic unit coupled with an IR sensor for the

short range. There is expansion ability for the suites to have plug-in gas sensors such as methane and carbon dioxide. The current design is slated for a single Nios II but the part size was chosen to allow for multiple processors. This action would allow for the sensors suites to be split if more intensive computation was required.

## Payload Processor (PP)

Payload Processor is the most versatile within the Master Controller, Figure 7. The PP could be the most under utilized or the hardest worked piece of silicon in the MC. The Payload Processor is simplistic in design, utilizing a single Nios II core that can be expanded to four Nios II processors. The PP does not have a configuration SEPROM on the module board; instead the SEPROM is located within the payload module. This allows for rapid field swapping of payloads with out the worry of handling configuration code or loading of an improper configuration.

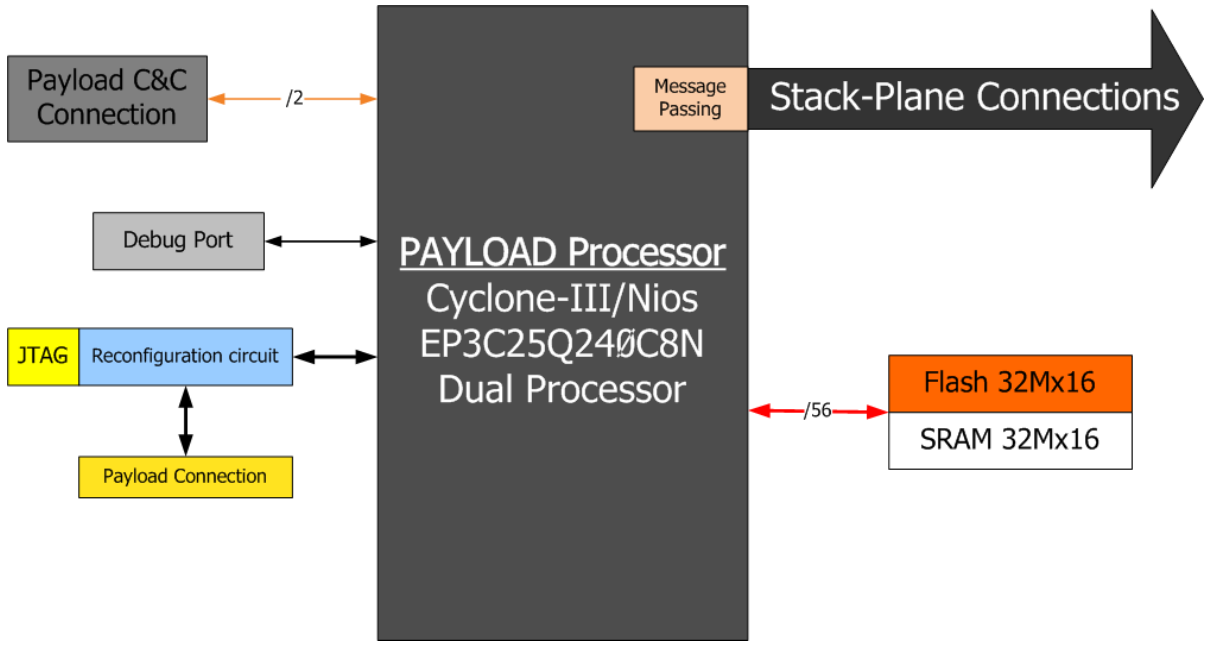


Figure 7 Payload Processor

The primary job of the Payload Processor is process control of the payload module. This could range from control of a 6-axis robotic arm to the simple function of controlling a single lift cylinder of a dump body.

Processor application code is also stored on the payload module, again allowing for ease of change out. Parameters that are required by the Master Processor are transferred after the Payload Processor has completely booted.

## Optional Systems

There are two optional systems for the SFARV and the other Omni-chassis's. Both of these units are in development stage.

### Light detection and ranging (LIDAR)

The LIDAR is the most commonly used external module on an ARV. These units use laser light to "paint" an image of what is in front of the sensor. This information can then be used to determine path and collision obstacles. The draw back for most companies is the cost per unit (around $6,000.00USD). A project is currently under way utilizing high speed CPLDs for the front end and a Cyclone III on the backend for graphic data extrapolation. The final outcome is to generate a low cost LIDAR and develop Intellectual Property (IP) that can be used in other CPLDs or FPGAs.

### Vision system

What ARV or robot is not complete without vision, at least to the Sci-fi people? Vision systems have a wide and varied use in robotics. For the SFARV and its brethren it is another tool for getting the job. The current project is for pattern recognition and basic color. The first application will be on the end of the wall constructing arm's end-effecter. The idea is to determine the position and color of the block, is it the correct block and which way do I twist my gripper to properly pick it up. The current test unit utilizes a single Cyclone III w/Nios II running at 120MHz. The processors primary job is data comparison. The project also tests doing the comparison in hardware. This advantage is in the compare speed.

## Locomotion System

The locomotion or drive system contains six hydraulically driven wheels. Each wheel is independently controlled via an intelligent proportional differential control valve. The valve controller receives information from the FOP on direction and rotational rate. The valve intelligence then controls the flow rate to the motor while monitoring the wheels actual revolution rate. The valve also keeps tabs on the line pressure to the motor. A wheel that can not keep its RPM steady or the pressure is outside of the preset parameters are immediately put into bypass mode. Bypass mode allows for the wheel to rotate with no power applied. A flag is also set in the motor controller indicating the loss or disabling of the wheel.

On the occasion that the SFARV is moving on an improved surface with a light payload one or two sets of wheels could be put into bypass conserving energy and system wear. Figure 8 contains the basic interconnection and drive system relationship.

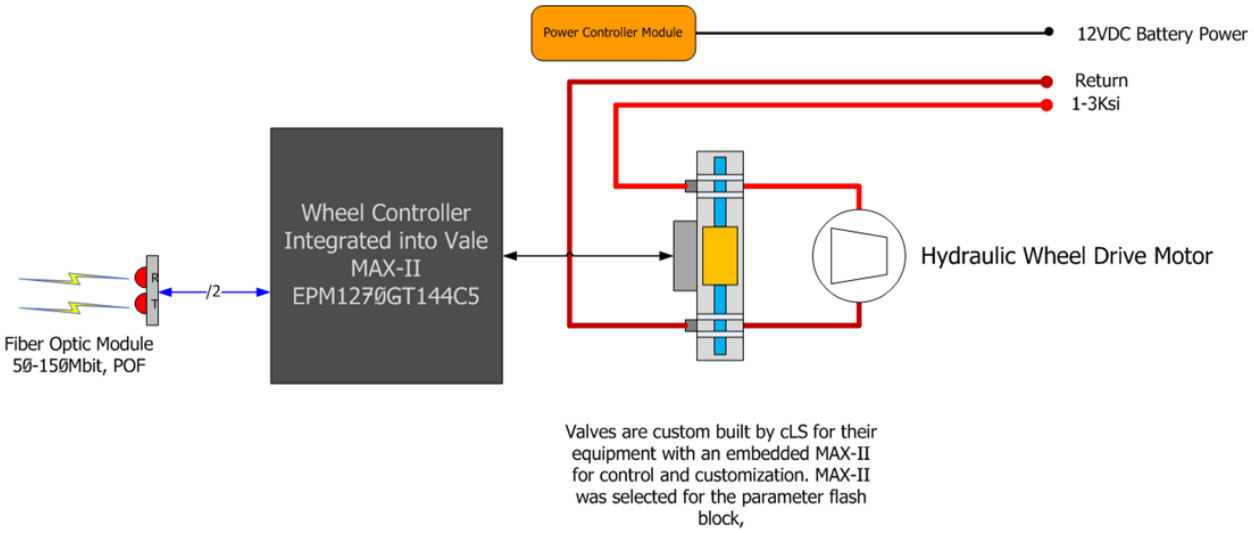


Figure 8 Wheel valve controller

## Battery monitor/pump control (BMPC)

The BMPC is the last system for review. This system is based on a pair of MAX IIGs. One unit handles the fiber optic communications and data parameter holding. The second unit does all the sensor data retrieval, parameter comparison and control output.

The primary functions of the duo are the control of the BLDC motor attached to the hydraulic pump, and the monitoring of the batteries (pack temperature, voltage and current). Pump control allows for power conservation, if pressure is not need, being parked idling, then the pump is slowed or stopped. The battery packs are monitored both during run time and charging. This is to prevent damage to the batteries.

## Related application notes

AN-1403: Distributive Multi-core Processing with a Single Cyclone III

AN-1404: Single FPGA based Guidance System

AN-1405: Multi-channel Fiber Optic Communication with a single FPGA

AN-1406: Message Passing with a Stack-Plane

AN-1407: Intelligent Hydraulic Valve Control with a CPLD

AN-1408: The FPGA/CPLD based LIDAR

AN-1409: FPGA base color/object recognition

## About the Author


| | |
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